Precision Analog Microcontroller, 12-Bit Analog I/O, Large Memory, ARM7TDMI MCU with Enhanced IRQ Handler

Silicon Anomaly

ADuC7124/ADuC7126

This anomaly list describes the known bugs, anomalies, and workarounds for the ADuC7124/ADuC7126 MicroConverter® Revision B silicon. The anomalies listed apply to all ADuC7124/ADuC7126 packaged material branded as follows:

First Line ADuC7124 or ADuC7126
Third Line B30

Analog Devices, Inc., is committed, through future silicon revisions, to continuously improve silicon functionality. Analog Devices tries to ensure that these future silicon revisions remain compatible with your present software/systems by implementing the recommended workarounds outlined here.

ADuC7124/ADuC7126 FUNCTIONALITY ISSUES

Silicon Revision Identifier	Kernel Revision Identifier	Chip Marking	Silicon Status	Anomaly Sheet	No. of Reported Anomalies
B	30	All silicon branded B30	Released	Rev. A	5

ADuC7124/ADuC7126 PERORMANCE ISSUES

Silicon Revision Identifier	Kernel Revision Identifier	Chip Marking	Silicon Status	Anomaly Sheet	No. of Reported Anomalies
B	30	All silicon branded B30	Released	Rev. A	2

FUNCTIONALITY ISSUES

Table 1. ADC Conversion—$\overline{CONV_{START}}$ Edge Trigger Mode [er001]

Background	ADC conversion can be set as $\overline{CONV_{START}}$ falling edge trigger mode by setting ADCCON Bit 13 and with ADCCON[2:0] = 000. Clearing ADCCON Bit 13 enables $\overline{CONV_{START}}$ high level trigger mode.
Issue	ADC conversion by $\overline{CONV_{START}}$ edge trigger mode is not reliable.
Workaround	Configure $\overline{CONV_{START}}$ through one PLA flip-flop with ULCK as its clock. This ensures that the ADC is triggered by $\overline{CONV_{START}}$ when its pulse width is more than 25 ns. This will be fixed in the next revision.
Related Issues	None.

Table 2. ADC Conversion—PLA Edge Trigger Mode [er002]

Background	The ADC conversion can be set as PLA rising edge trigger mode by setting ADCCON Bit 13 and with ADCCON[2:0] = 101. Clearing ADCCON Bit 13 enables PLA low level trigger mode.
Issue	ADC conversion by PLA edge trigger mode is not reliable.
Workaround	Configure the PLA element output through another PLA flip-flop with ULCK as its clock. This ensures that the ADC is triggered by the PLA edge when CD is less than 5. This will be fixed in the next revision.
Related Issues	None.

Table 3. Disabling I^2C Interface in Slave Mode When a Transfer Is in Progress [er003]

Background	The I2CSEN bit (Bit 0 in the I2CxSCON register) enables/disables the I^2C slave interface. The I2CSBUSY bit (Bit 6 in the I2CxSSTA register) indicates whether the I^2C slave interface is busy.
Issue	If I^2C slave mode is enabled (I2CxSCON Bit 0 = 1) and a transfer is in progress with the master, do not clear I2CxSCON Bit 0 to 0 to disable the I^2C slave interface until the I^2C busy bit, I2CSBUSY (Bit 6 of I2CxSSTA), is cleared. When I2CxSCON Bit 0 is cleared to 0 and I2CSBUSY is still set, the ADuC7124/ADuC7126 may drive the SDAx pins low indefinitely. When this condition occurs, the ADuC7124/ADuC7126 do not release the SDAx pins unless a hardware reset condition occurs.
Workaround	When disabling I^2C slave mode by writing to the I2CSEN bit (Bit 0 in the I2CxSCON register), first set the I2CMEN bit (Bit 0 in the I2CxMCON register) = 1 to enable master mode. Then disable the slave mode by clearing the I2CSEN bit. Finally, clear the I2CMEN bit.
Related Issues	None.

Table 4. Operation of SPI in Slave Mode [er004]

Background	When in SPI slave mode, the ADuC7124/ADuC7126 expect the number of clock pulses from the master to be divisible by 8 when the chip select ($\overline{CS}$) pin is low. The internal bit shift counter within the ADuC7124/ADuC7126 is not reset when the chip select pin is deasserted.
Issue	If the number of clocks from the master is not divisible by 8 when the chip select is active, incorrect data may be received or transmitted by the ADuC7124/ADuC7126 because the bit shift counter will not be at 0 for future transfers. The internal bit shift counter for the transmit or receive buffers can only be reset by a hardware, software, or watchdog reset.
Workaround	Always ensure that the number of SPI clocks is divisible by 8 when the ADuC7124/ADuC7126 chip select is active.
Related Issues	None.

Table 5. Timer0 in Periodic Mode with Internal 32 kHz Clock [er005]

Background	In periodic mode, the internal counter decrements/increments from the value in the load register (T0LD MMR) until zero/full scale and starts again at the value stored in the load register. The value of a counter can be read at any time by accessing its value register (T0VAL).
Issue	The first timer interrupt occurs only after a full 16-bit countdown. After the countdown, the T0LD value is copied into T0VAL as expected. This issue occurs only when the 32 kHz oscillator is serving as the timer source.
Workaround	None.
Related Issues	None.

PERFORMANCE ISSUES

Table 6. ADC and DAC Reference Selection Limitation [pr001]

Background	The ADuC7124/ADuC7126 provide an on-chip band gap reference of 2.5 V, which can be used for the ADC and DACs. This internal reference also appears on the V_{REF} pin. When using the internal reference, a 0.47 µF capacitor must be connected from the external V_{REF} pin to AGND to ensure stability and fast response during ADC conversions.
Issue	When REFCON = 0x00 is set, the internal 2.5 V reference is unstable; that is, when the ADC uses the external reference (REFCON = 0x00) and the DACs use the internal 2.5 V reference (DACxCON[1:0] = 10), the DAC output is unstable.
Workaround	Set REFCON = 0x00 for the ADC to use the external reference, and set DACxCON[1:0] = 01 for the DACs to use a different external reference from DAC_{REF}.
Related Issues	None.

Table 7. JTAG Clock Limitation [pr002]

Background	The JTAG clock speed is limited.
Issue	JTAG speed requires TCK < UCLK/($2^{CD} \times 6$); that is, TCK should be changed according to how the CD (CPU clock divider) bits are set. If TCK is greater than the limitation, the JTAG cannot download until the power-on reset (POR) is at the correct TCK speed.
Workaround	The JTAG clock speed must be set up manually. The default kernel setting for the CPU clock is CD = 3 (5.22 MHz). Therefore, a JTAG clock speed limitation of 800 kHz or less must be maintained.
Related Issues	None.

SECTION 1. ADuC7124/ADuC7126 FUNCTIONALITY ISSUES

Reference Number	Description	Status
er001	ADC conversion—$\overline{\text{CONV}_{\text{START}}}$ edge trigger mode	Open
er002	ADC conversion—PLA edge trigger mode	Open
er003	Disabling I^2C interface in slave mode when a transfer in progress	Open
er004	Operation of SPI in slave mode	Open
er005	Timer0 in periodic mode with an internal 32 kHz clock	Open

SECTION 2. ADuC7124/ADuC7126 PERFORMANCE ISSUES

Reference Number	Description	Status
pr001	ADC and DAC reference selection limitation	Open
pr002	JTAG clock limitation	Open

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